Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 02986.P028	Application Number: 10/626,031
	First Named Inventor: Kenneth S. McElvain	
	Filing Date: July 23, 2003	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (If known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

OTHER ART – NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation[2]
/S.C./		Magma Design Automation, Inc., "Deep-Submicron Signal Integrity", white paper, 2002	
/S.C./		Andrey V. Mezhiba, Eby G. Friedman, "Scaling Trands of On-Chip Power Distribution Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.47-53	
/S.C./		Sani R. Nassif, Onsi Fakhouri, "Technology Trends in Power-Grid-Induced Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.55-59	
/S.C./		Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim, "Analytical Signal Integrity Verification Models for Inductance-Dominant Multi-Coupled VLSI Interconnects", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.61-68	
/S.C./		S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten, "A novel VLSI layout fabric for deep sub-micron applications," in *Proceedings of the Design Automation Conference*, (New Orleans), June 1999.	
/S.C./		Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Immune VLSI Design using a Network of PLAs Embedded in a Regular Layout Fabric", IEEE/ACM International Conference on Computer Aided Design, ICCAD-2000, November 5-9, 2000, San Jose, CA, USA	

Examiner Signature	/Sheila Clark/	Date Considered	08/31/2010

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.